

WHAT IS CLAIMED IS:

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1. A semiconductor device including:  
a semiconductor substrate having a main surface;  
a semiconductor layer of a first conductive type which is formed on  
the main surface of said semiconductor substrate;  
5 a first buried impurity region of the first conductive type formed  
between said semiconductor layer and said semiconductor substrate;  
a second buried impurity region of a second conductive type formed  
between said first buried impurity region and said semiconductor layer;  
10 a first impurity region of the second conductive type which is formed  
in the surface of said semiconductor layer and which is electrically  
connected to said second buried impurity region;  
a second impurity region of the first conductive type which is formed  
in the surface or inside of said semiconductor layer located in a region  
15 above said second buried impurity region; and  
a semiconductor element which includes said first impurity region  
and said second impurity region and which has a switching function formed  
on the surface of said semiconductor layer,  
20 wherein the withstand voltage is secured by a depletion layer  
extending from an interface between said second buried impurity region  
and said semiconductor layer under the condition where said  
semiconductor element is turned OFF; and  
25 said second buried impurity region includes a first recessed part  
wherein a surface of said second buried impurity region is recessed in the  
direction away from said second impurity region in a part located,  
approximately, directly beneath said second impurity region or a first gap  
part wherein said second buried impurity region is disconnected.
2. The semiconductor device according to claim 1, wherein said  
semiconductor element includes:  
a third impurity region of the first conductive type formed on the  
surface of said first impurity region so as to be surrounded by said first

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5 impurity region; and  
an electrode part formed on the surface of said first impurity region  
sandwiched between said third impurity region and said semiconductor  
layer with an insulating film interpolated in between.

3. The semiconductor device according to claim 2, wherein said  
semiconductor element further includes a fourth impurity region of the  
second conductive type which is formed so as to contact with said second  
impurity region.

4. The semiconductor device according to claim 1, wherein said  
semiconductor element includes a fifth impurity region of the second  
conductive type which is formed on a surface of said semiconductor layer.

5. The semiconductor device according to claim 1, wherein said  
second buried impurity region includes a plurality of said first recessed  
parts.

6. The semiconductor device according to claim 1, wherein said  
second buried impurity region includes a plurality of said first gap parts.

7. The semiconductor device according to claim 6, wherein said  
second buried impurity region includes a plurality of regions which are,  
respectively, made to be in an electrically floating condition by a plurality  
of said first gap parts.

8. The semiconductor device according to claim 1, wherein said first  
buried impurity region includes a second recessed part wherein a surface of  
said first buried impurity region is recessed in the direction away from said  
second impurity region in a part located, approximately, directly beneath  
said first gap part or a second gap part wherein said first buried region is  
disconnected.

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9. The semiconductor device according to claim 4, wherein a junction interface between said first buried impurity region and said second buried impurity region is uneven.

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5 10. A semiconductor device including:  
a semiconductor substrate having a main surface;  
a semiconductor layer of a first conductive type formed on the main surface of said semiconductor substrate;  
a buried impurity region of the first conductive type formed between said semiconductor substrate and said semiconductor layer;  
a first impurity region of the first conductive type which is formed on the surface of said semiconductor layer and which is electrically connected to said buried impurity region;

10 15. a second impurity region of a second conductive type formed on a surface of said semiconductor layer located in a region above said buried impurity region; and  
a semiconductor element which includes said first impurity region and said second impurity region and which has a switching function formed on the surface of said semiconductor layer,  
wherein a withstand voltage is secured by a depletion layer extending from an interface between said second impurity region and said semiconductor layer under the condition where said semiconductor element is turned off; and

20 said buried impurity region includes a recessed part wherein a surface of said buried impurity region is recessed in the direction away from said second impurity region in a part located, approximately, directly beneath said second impurity region or a gap part wherein said buried region is disconnected.

11. The semiconductor device according to claim 10, wherein said semiconductor element includes:

a third impurity region of the first conductive type formed on a surface of said second impurity region so as to be surrounded by said

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second impurity region; and  
an electrode part formed on a surface of said second impurity region  
sandwiched by said third impurity region and said semiconductor layer  
with an insulating film interpolated in between.

12. The semiconductor device according to claim 10, wherein said  
semiconductor element includes a fourth impurity region of the second  
conductive type formed on a surface of said semiconductor layer.

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13. The semiconductor device according to claim 10, wherein said  
recessed part or gap part is formed in a part that is in the direction to  
which said depletion layer extends.